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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THOMPSON, JAMES A	
ART UNIT	**PAPER NUMBER**
2624	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,147	GESNOT, ARNAUD	
	Examiner	Art Unit	
	James A. Thompson	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 30 September 2005 have been fully considered but they are not persuasive.

Regarding page 4, lines 10-22: Applicant's prior arguments dated 09 March 2005 with respect to the claim step of "computing mask values" were fully addressed by Examiner in the subsequent Advisory Action dated 11 March 2005 and mailed 18 March 2005 and the previous office action, dated 02 June 2005 and mailed 30 June 2005. A proposed amendment to the claimed step of "computing mask values" was presented, and later entered after the filing of a Request for Continued Examination on 11 April 2005. Applicant's arguments of 09 March 2005 were directed to an amendment to the claims. Since said amendment changed the overall scope of the claims and overcame the prior art rejections previously presented, the proper response was fully given in the new grounds of rejection presented in said previous office action. In fact, a simple reading of said previous office action makes abundantly clear that Examiner has agreed with Applicant that Moronaga (US Patent 5,229,864) does not fully teach the step of "computing mask values" as fully recited in present claim 1. Examiner has fully demonstrated that the combination of Moronaga in view of Yamada (US Patent 5,953,461) does teach the step of "computing mask values" as fully recited in present claim 1 [see item 3 of said previous office action].

Regarding page 5, lines 1-11: Examiner has *not* cited column 4, lines 11-16 of Moronaga to teach the claimed "correction area corresponding to an area where the mask values are different from zero." Examiner has cited column 11, lines

21-27 of Moronaga to teach said correction area [see page 3, lines 7-9 of said previous office action]. Column 11, lines 21-27 of Moronaga clearly teaches said recited correction area. Additionally, a further explanation with respect to column 11, lines 21-27 of Moronaga is given on page 3, lines 13-26 of said previous office action.

Regarding page 5, lines 12-20: Moronaga clearly teaches mask values, as set forth on page 3, lines 4-26 of said previous office action. Applicant has provided no substantive arguments, but merely alleges that mask values are not taught. Further, the manner in which Moronaga and Yamada are combined, along with adequate motivation, are given on page 4, lines 7-21 of said previous office action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moronaga (US Patent 5,229,864) in view of Yamada (US Patent 5,953,461).

Regarding claim 1: Moronaga discloses a method of processing an input signal (column 3, lines 36-37 of Moronaga), said input signal comprising said blocks (column 3, lines 37-39 of Moronaga). Said blocks comprise pixels of digital picture

data (column 3, lines 36-39 of Moronaga), which, by the definition of digital pixels, must be n-bit binary input samples, with n being an integer.

Moronaga further discloses a low pass filtering step applied to the input signal (figure 12(300) and column 11, lines 21-23 of Moronaga), which results in a filtered signal comprising filtered samples (column 11, lines 23-27 of Moronaga); and a determination step (figure 12(18) of Moronaga) for determining a correction area around block boundaries (column 4, lines 9-16 of Moronaga), said determination step including computing mask values (column 11, lines 21-23 of Moronaga) associated with the input samples (column 11, lines 23-27 of Moronaga), said correction area corresponding to an area where the mask values are different from zero (column 11, lines 21-27 of Moronaga). The combining section (figure 12(18) of Moronaga) combines 8x8 pixel blocks (column 4, lines 9-10 of Moronaga), thus defining a correction area, for correcting distortion between nearby blocks (column 4, lines 11-16 of Moronaga). A low-pass filter is used for correction of the correction area (column 11, lines 21-23 of Moronaga). As is well-known in the art, a low-pass image filter filters the image pixel data over an area. In Moronaga, the area is the correction area. Since the low-pass filtering is performed based on the activity of the correction area (column 11, lines 23-27 of Moronaga), the mask values of the low-pass filter are therefore associated with the input samples. Since, as is well-known in the art, low-pass filters distinguish between high frequency components and low frequency components and pass the low frequency components, said low-pass filter must inherently have mask values that are non-zero. Otherwise, there is no

distinguishing between low frequency components and high frequency components.

Moronaga further discloses a correction step for adding a random binary number (figure 12(302) of Moronaga) comprising at least one bit to the filtered samples belonging to the correction area, which results in an output signal (column 12, lines 50-53 of Moronaga). Said random noise inherently comprises at least one bit in order to exist as an actual digital number.

Moronaga does not disclose expressly that the mask values associated with the input samples are computed using the filtered samples.

Yamada discloses using a low pass filter (figure 1(11) of Yamada) to obtain filtered values (figure 1(Sus) and column 11, lines 53-59 of Yamada) which are then used to compute mask values (Sorg-Sus) associated with the input samples (Sorg) (column 11, lines 59-63 and column 12, lines 11-14 of Yamada).

Moronaga and Yamada are combinable because they are from the same field of endeavor, namely filtering image data signals in order to reduce image artifacts. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use the low-pass filter values to obtain the mask values, as taught by Yamada. The motivation for doing so would have been to emphasize an edge portion of the image (column 7, lines 10-16 and column 11, lines 48-52 of Yamada). Therefore, it would have been obvious to combine Yamada with Moronaga to obtain the invention as specified in claim 1.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moronaga (US Patent 5,229,864) in view of Yamada (US Patent 5,953,461) and Jung (US Patent 5,732,159).

Regarding claim 2: Moronaga discloses applying a filtering step (figure 12(300) of Moronaga) to the signal input into said filtering step block (column 11, lines 21-23 of Moronaga) around block boundaries (column 11, lines 25-29 of Moronaga); and adding a random binary number to the filtered samples that are input into the random noise addition block (column 11, lines 30-35 of Moronaga), which results in an output signal (column 11, lines 37-39 and lines 44-45 of Moronaga).

Moronaga in view of Yamada does not disclose expressly multiplying the input samples by a power of 2, which results in a modified signal comprising modified samples of m-bit binary numbers; a computing sub-step of mask values equal to the m-n least significant bits of the filtered samples; dividing the filtered samples by said power of 2; and specifically executing said step of adding a random binary number after said filtered samples have been divided by said power of 2 and when the mask values are different from zero.

Jung discloses multiplying the input samples by a power of 2 (figure 2; and column 2, equation 1 and lines 56-61 of Jung). Since the filtered binary number represents fractional values, said fractions being ¼, ½ or ¾ (figure 2; figure 3B and column 2, lines 56-61 of Jung), two more bits are needed to represent said numbers, said bits being the two least significant bits. As a pure binary number, and thus representing a binary integer, the modified values are multiplied by four when two extra bits are added, and then a value of 00 (binary), 01(binary), 10 (binary) or 11 (binary) is added or subtracted (figures 3A-3B

and column 2, lines 58-61 of Jung). Therefore, said step of multiplying results in a modified signal comprising modified samples of m-bit numbers. For the purpose of greater clarity, an example is given below. Said example is taken from the alterations made to the input signal shown in figure 3A, which are reflected in the output shown in figure 3B, particularly the column above the "1" in "14" in both of said figures. Said column from figure 3A-3B displays a value that is altered from 126 to 125.75.

126 (decimal) written as a binary number is 1111110 (binary). 125.75 written as a binary number is 1111101.11 (binary). However, since there are no decimal points in a real computer binary representation, the pure binary number used to represent 125.75 is 111110111 (binary), which translates to an equivalent decimal value of 503. 126 (decimal) written as a binary number using the same number of representative bits is written as 1111110.00 (binary), which taken as a pure binary number is 111111000 (binary), which translates to 504 (decimal). The binary representation of 126.00 (decimal) as a pure binary number using the same number of bits as 125.75 (decimal), is a binary number four times the value of the original, unaltered representation of 126 (decimal).

The difference signal (figure 3C and column 2, lines 62-67 of Jung), which corresponds to the least significant (m-n) bits, denotes the region of discontinuity between image blocks (column 3, line 67 to column 4, line 4 of Jung), and thus the area that needs to be corrected.

Moronaga in view of Yamada is combinable with Jung because they are from the same field of endeavor, namely filtering image data signals in order to reduce image artifacts. At the time of

the invention, it would have been obvious to a person of ordinary skill in the art to use the filtering method and increased number of representative bits to determine the region of discontinuity between image blocks, as taught by Jung. Said determination would then be used in correction area determination performed by Moronaga. Said random binary numbers would then be added to the resultant pixel values. Since the output of Moronaga is limited to a range of 0 to 255 to represent the image (column 11, lines 40-44 of Moronaga), and thus eight bits, the random number would therefore be added to an 8-bit number (column 11, lines 41-42 of Moronaga). Therefore, with an output of eight bits, the two least significant bits representing the fraction of the pixel value would be dropped, thus dividing the pure binary number by a factor of four using the same logic discussed above. The motivation for doing so would have been to reduce blocking effects (column 1, lines 35-37 of Jung). Therefore, it would have been obvious to combine Jung with Moronaga in view of Yamada to obtain the invention as specified in claim 2.

5. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moronaga (US Patent 5,229,864) in view of Yamada (US Patent 5,953,461) and Nakaya (US Patent 6,295,376 B1).

Regarding claim 3: The arguments regarding claim 1 are incorporated herein. Moronaga in view of Yamada discloses a computer program product (figure 12 of Moronaga) that comprises a set of instructions that, when loaded, carries out the method of claim 1 (column 11, lines 10-11 and lines 16-20 of Moronaga). The embodiment of the invention shown in figure 12 of Moronaga

is used to correct distortion in digital pixel data (column 11, lines 16-20 of Moronaga). Some form of computer program product embodied in some form of computer memory is required to process said digital pixel data, each of the sections of the embodiment in figure 12 of Moronaga comprising a section of the computer program product.

Moronaga in view of Yamada does not disclose expressly that said computer program product is for a television receiver and is loaded into a television receiver.

Nakaya discloses installing an image processing device into a television receiver (column 12, lines 15-17 of Nakaya).

Moronaga in view of Yamada is combinable with Nakaya because they are from the same field of endeavor, namely video image data processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to install the computer program product of Moronaga in view of Yamada into a television receiver and use said computer program product for said television receiver, as taught by Nakaya. The motivation for doing so would have been to have the computer programming product in a device that is capable of receiving and displaying digital image data (column 12, lines 27-31 of Nakaya). Therefore, it would have been obvious to combine Nakaya with Moronaga in view of Yamada to obtain the invention as specified in claim 3.

Regarding claim 4: The arguments regarding claim 1 are incorporated herein. Moronaga in view of Yamada discloses a computer program product (figure 12 of Moronaga) that comprises a set of instructions that, when loaded, carries out the method of claim 1 (column 11, lines 10-11 and lines 16-20 of Moronaga). The embodiment of the invention shown in figure 12 of Moronaga

is used to correct distortion in digital pixel data (column 11, lines 16-20 of Moronaga). Some form of computer program product embodied in some form of computer memory is required to process said digital pixel data, each of the sections of the embodiment in figure 12 of Moronaga comprising a section of the computer program product.

Moronaga in view of Yamada does not disclose expressly that said computer program product is for a set-top-box and is loaded into a set-top-box.

Nakaya discloses installing an image processing device into a set top box (column 12, lines 21-23 of Nakaya).

Moronaga in view of Yamada is combinable with Nakaya because they are from the same field of endeavor, namely video image data processing. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to install the computer program product of Moronaga in view of Yamada into a set top box and use said computer program product for said set top box, as taught by Nakaya. The motivation for doing so would have been to have the computer programming product in a device that is capable of receiving and displaying digital image data (column 12, lines 27-31 of Nakaya). Therefore, it would have been obvious to combine Nakaya with Moronaga in view of Yamada to obtain the invention as specified in claim 4.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James A. Thompson whose telephone number is 571-272-7441. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David K. Moore can be reached on 571-272-7437. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James A. Thompson
Examiner
Art Unit 2624

26 November 2005

THOMAS D.